REMARKS

Claims 1, 3, 4, 9, 11, 12 and 16-25 are pending in the present application, were examined, and stand rejected. In response, Claims 9 and 16 are amended, Claims 1, 3 and 4 are cancelled and no claims are added. Applicant respectfully requests reconsideration of pending Claims 9, 11, 12 and 16-25 in view of at least the following remarks. Reconsideration and withdrawal of the rejections of record are requested in view of such amendments and the following discussion.

I. Claims Rejected Under 35 U.S.C. §112

The Examiner has rejected Claims 1, 3-9 and 11-12 under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement.

Regarding Claims 1 and 9, Claims 1 and 9 are amended to remove reference to an off-chip system memory.

Accordingly, Applicant respectfully submits that in view of Applicant's amendments to Claims 1 and 9, Claims 1, 3-4, 9 and 11-12 comply with the written description requirement under 35 U.S.C. §112, first paragraph. Accordingly, Applicant respectfully requests the Examiner reconsider and withdraw the 35 U.S.C. §112, first paragraph rejection of Claims 1, 3-4, 9 and 11–12.

II. Claims Rejected Under 35 U.S.C. §102

The Examiner has rejected Claims 20-22 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,128,702 issued to Saulsbury et al. ("Saulsbury"). Applicant respectfully traverses this rejection.

Applicant respectfully asserts that the Patent Office has failed to adequately set forth a *prima facie* rejection under 35 U.S.C. §102(b). "Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, *arranged as in the claim.*" *Lindemann Maschinenfabrik v. American Hoist & Derrick* ("Lindemann"), *730 F.2d 452, 1458 (Fed. Cir. 1994)* (emphasis added). Additionally, each and every element of the claim must be exactly disclosed in the anticipatory reference. *Titanium Metals Corp. of American v. Banner* ("Banner Titanium"), *778 F.2d 775, 777 (Fed. Cir. 1985).*

Regarding Claim 20, Claim 20 recites the following claim feature, which is neither disclosed nor suggested by Saulsbury or the references of record:

> the memory module to receive a writeback command, the writeback command to cause a previous line of data, evicted from the data cache and stored within the eviction buffer, to be written out of the eviction buffer to the memory device. (Emphasis added.)

According to the Examiner, the above-recited feature of Claim 20 is disclosed by Saulsbury at col. 11, line 47 - col. 12, line 16 and col. 12, line 48 - col. 13, line 66. (*See*, pg. 3, ¶4 of Final

Office Action mailed March 24, 2005.) After having carefully reviewed the passages cited by the Examiner, as well as the entire specification of Saulsbury, Applicant respectfully disagrees with the Examiner's contention.

According to the Examiner, Saulsbury discloses a victim data cache, which is similar to the eviction buffer, as recited by Claim 20. As defined by Saulsbury:

> the victim data cache is used to store victim data cache sub-lines (or sub-blocks) of primary data cache lines that were recently replaced (i.e., were replacement victims) with new primary data cache lines in the primary data cache banks 122. (col. 8, lines 5-9.) (Emphasis added.)

However, in contrast to the above-recited features of Claim 20, Saulsbury explicitly requires that any writes to main memory bank 118 must be performed from the primary data cache banks 122. In other words, as described within Saulsbury, the writing of data to main memory banks 110 is performed from the primary cache banks 122 and not from the victim data cache 106, as recited by Claim 20. As described within Saulsbury:

> prior to replacing the victim data cache line with a new data cache line, the primary data cache bank controls state machine 152 writes back to the corresponding main memory bank 118 the victim primary data cache line if it is dirty (state 163 of FIG. 6) . . . If it is dirty, then the primary data cache bank control state machine issues on the control bus 116 a dirty cache line write signal indicating that it needs to write back a dirty victim primary cache line. (col. 12, lines 48-60.) (Emphasis added.)

Based on the cited passage above, Applicant respectfully submits that the Examiner has inappropriately equated the victim data cache lines, as taught by Saulsbury, with the victim data cache sub-lines, or sub-blocks, that are stored within the victim data cache 106. Based on the cited passages above, the capacity of the victim data cache 106 taught by Saulsbury prohibits the storage of an entire victim data cache line. Consequently, it is not possible for a victim data cache line to be written from victim data cache 106 to main memory bank 118, as suggested by the Examiner.

Hence, Saulsbury is expressly limited to the writing of the victim data cache lines, which are contained within the primary data cache banks 122, from the primary data cache banks 122 to the main memory bank 118 prior to replacement by a new data cache line. (*See*, col. 12, lines 48–60.)

Furthermore, as shown in FIG. 9 of Saulsbury, the victim cache control state machine 168 illustrates that access to data within the victim data cache 106 is limited to situations where a victim data cache hit is detected during issuance of a read signal from CPU 102. In other words, as explicitly recited by Saulsbury:

> When the W/R signal indicates that a read is occurring and the victim data cache hit/miss signal indicates that a victim data cache hit has occurred, then the victim data cache control state machine leaves its idle state (state 171 of FIG. 9) and decodes the received 6 address bits to determine the accessible memory location of the data word in the identified victim data cache sub-line at which the data word is to be read. The victim data cache control state machine then reads the data word from

> the identified victim data cache sub-line and provides it to the CPU 102 (state 173 of FIG. 9.). (col. 9, lines 13-23.) (Emphasis added.)

Consequently, Applicant respectfully submits that the writing of victim data cache lines from the primary data cache banks 122 to corresponding main memory banks 118, as described by Saulsbury in the passages cited by the Examiner (*see*, col. 11, line 47 - col. 12, line 6 and col. 12, lines 48 - col. 13, line 66) fails to disclose the writing of data stored within an eviction buffer to a memory device, as recited by Claim 20. However, the case law is clear in establishing that anticipation requires the presence of each and every element as exactly disclosed by the claim within an anticipatory reference. Id.

Accordingly, Applicant respectfully submits that the Examiner has failed to establish a *prima facie* case of anticipation of Claim 20, since the Examiner is prohibited from relying on Saulsbury as an anticipatory reference since Saulsbury fails to disclose the writing of data from an eviction buffer to a memory device, as recited by Claim 20. Id.

Therefore, Applicant respectfully submits that Claim 20 is patentable over Saulsbury, as well as the references of record. Consequently, Applicant respectfully submits that the Examiner reconsider and withdraw the §102(b) rejection of Claim 20.

Regarding Claims 21 and 22, Claims 21 and 22, based on their dependency from Claim 20, are also patentable over Saulsbury, as well as the references of record. Consequently, Applicant respectfully submits that the Examiner reconsider and withdraw the §102(b) rejection of Claims 21 and 22.

III. Claims Rejected Under 35 U.S.C. §103

The Examiner has rejected Claims 1, 3, 4, 9, 11-12, 16-19 and 23-25 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,216,178 issued to Stracovsky et al. ("Stracovsky") in view of Saulsbury. Applicant respectfully traverses this rejection.

To establish a *prima facie* case of obviousness, the following criteria must be met: (1) there must be some suggestion or motivation to modify the reference or combine the reference teachings, (2) there must be a reasonable expectation of success, and (3) the prior art references must teach or suggest all the claim limitations. (MPEP §2142) For the reasons provided below, the Examiner has failed to establish a *prima facie* case of obviousness in view of the references of record.

Regarding Claim 9, Claim 9, as amended, recites:

> a system memory coupled to the memory controller, the system memory including at least two memory modules, each memory module including
>
> at least one memory device, and
>
> a data cache coupled to an eviction buffer, each coupled to the memory device, the data cache controlled by a plurality of commands delivered by the memory controller, the memory controller writing a current line of data to the data

> cache, the memory controller to further instruct the data cache to evict a previous line of data from the data cache into the eviction buffer. (Emphasis added.)

Applicant respectfully submits that neither the combination of Stracovsky in view of Saulsbury, or the references of record, disclose a system memory including at lest two memory modules, each memory module including at least one memory device having a data cache and an eviction buffer, as recited by amended Claim 8.

Hence, amended Claim 9 recites a data cache and an eviction buffer per memory module of a system memory, which includes at least two memory modules. Conversely, the integrated PM device 100, as taught by Saulsbury, includes:

> an on-chip system memory . . . The memory system including 16 memory blocks 104 and a victim cache 106. (col. 3, lines 46-53.) (Emphasis added.)

Consequently, Applicant respectfully submits that the combination of Stracovsky in view of Saulsbury teaches a single victim data cache for the entire system memory (*see*, col. 3, lines 46-53); and hence, fails to disclose a system memory including at least two memory modules where each memory module includes at least one memory device, a data cache and an eviction buffer, each coupled to the memory device, as recited by amended Claim 9.

Therefore, Applicant respectfully submits that Claim 9, as amended, is patentable over the combination Stracovsky in view of Saulsbury. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claim 9, as amended.

Regarding Claims 11 and 12, Claims 11 and 12, based on their dependency from Claim 9, as amended, are also patentable over the combination Stracovsky in view of Saulsbury, as well as the references of record Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 11 and 12.

Regarding Claim 16, Claim 16 is amended to recite the following claim feature, which is neither taught nor suggested by the combination of Stracovsky in view of Saulsbury or the references of record:

> a command sequencer and serializer unit coupled to the array of tag address storage locations, the command sequencer and serializer unit to control a data cache and an eviction buffer located on at least one memory module of a system memory, the command sequencer and serializer to deliver a writeback command to the eviction buffer associated with the memory module, the writeback command to cause a previous line of data evicted from the data cache and stored in the eviction buffer, to be written out of the eviction buffer to a memory device of the memory module. (Emphasis added.)

For at least the reasons indicated above with reference to Claim 20, the teachings of Saulsbury are expressly limited to writing back a victim data cache line from primary data cache bank 122 to main memory bank 118 prior to replacement of the victim data cache line with a new data cache line if the victim data cache line is dirty. (*See*, col. 12, lines 48-60.) In other words, any

writes to main memory bank 118, as taught by Saulsbury, are performed from primary cache banks 122. As a result, data is not read from victim data cache 106 and written to main memory banks 118, as would be required to teach or suggest the above-recited features of amended Claim 16.

Furthermore, as explicitly disclosed by Saulsbury, access to data within victim data cache 106 is limited to situations where a victim data cache hit is detected during issuance of a read signal by CPU 102, which results in a transition from state 171 of FIG. 9 to state 173 of FIG. 9, wherein data is read from the victim data cache sub-line and provided to CPU 102. (*See*, col. 9, lines 13–23.)

Accordingly, Applicant respectfully submits that Applicant's amendments to Claim 16 prohibit the Examiner from establishing a *prima facie* case of obviousness of amended Claim 16, since the combination of Stracovsky in view of Saulsbury fails to teach or suggest the write-back command, as recited by amended Claim 16, to cause evicted data contained with an eviction buffer to be written out of the eviction buffer to a memory device of a memory module.

Therefore, Applicant respectfully submits that Claim 16, as amended, is patentable over the combination of Stracovsky in view of Saulsbury, as well as the references of record. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claim 16.

Regarding Claims 17-19, Claims 17-19, based on their dependency from Claim 16, as amended, are also patentable over the combination of Stracovsky in view of Saulsbury, as well as the references of record. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 17-19.

Regarding Claim 23, Claim 23 recites

> A system memory comprising:
> at least two memory modules, each memory module including:
> at least one memory device, and
> a data cache coupled to an eviction buffer, each coupled to the memory device. (Emphasis added.)

In contrast to the above-recited features of Claim 23, the integrated PM device 100, as taught by Saulsbury, includes:

> an on-chip system memory . . . The memory system including 16 memory blocks 104 and a victim cache 106. (col. 3, lines 46-53.)

Based on the cited passage above, Saulsbury teaches that the integrated memory system 103 includes 16 memory blocks and a single victim cache 106. Conversely, Claim 23 recites a data cache and an eviction buffer per memory module of a system memory, which includes at least two memory modules.

Consequently, Applicant respectfully submits that the combination of Stracovsky in view of Saulsbury teaches a single victim data cache for the entire system memory; and hence, fails to

disclose a system memory including at least two memory modules where each memory module includes at least one memory device, a data cache and an eviction buffer, each coupled to the memory device, as recited by Claim 23.

Consequently, Claim 23 is patentable over the combination of Stracovsky in view of Saulsbury, as well as the references of record. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claim 23.

Regarding Claims 24 and 25, Claims 24 and 25, based on their dependency from Claim 23, are also patentable over the combination of Stracovsky in view of Saulsbury, as well as the references of record. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 24 and 25.

CONCLUSION

In view of the foregoing, it is submitted that Claims 9, 11 12 and 16-25, as amended, patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,
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Dated: June 3, 2005

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CERTIFICATE OF FACSIMILE:
I hereby certify that this correspondence is being transmitted via facsimile on the date shown below to the United States Patent and Trademark Office.

_____
Marilyn Bass June 03, 2005